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Dr. Choi is a VP of Technology in the Process Development at Samsung Electronics. He received the Ph.D. degree in the department of Materials Science and Engineering from KAIST in 1999. Since joining Samsung Electronics' Semiconductor R&D Center in 1999, he has been involved in working on the next-generation atomic layer deposition & treatment processes, equipment & materials for memory devices.

He is currently leading the R&D of various thin film deposition and treatment processes for Charge Trap Flash in VNAND devices. His current research interests mainly focus not only on new materials & fabrication techniques for advanced Charge Trap Flash modules, but also on electrical characterization and modeling related to device performance and reliability.