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Chanmin Lee is a master (VP of Technology) of Etch process at Samsung Electronics and leads the DRAM FEOL & MEOL etching process development in R&D center. He received BS, MS, and Ph.D degrees in nuclear engineering from Seoul National University and started career as an etch engineer at Samsung in 2008. Since joining Samsung, he has been involved in developing the etch process for the next generation DRAM devices. His major contributions include the HART (high Aspect ratio trench) etching process and integration design for DRAM FEOL & MEOL module. His current research interests mainly focus on developing the technologies to overcome the etching limitations such as ALE and low damage process.