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KISM 2024 BUSAN

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Today I lead the research activity of DOT department (Design, OPC and mask Tape out). Since few years, I chair imec conference about Patterning DTCO. This conference covers printability and design aspects for advanced nodes in both Logic and DRAM from the perspective of printability, yield, and path finding topics such as curvilinear design and OPC.
Muy career at imec, Belgium started in Silicon Photonics in 2009. I have developed 1st hand expertise in verification for curvilinear designs. IN 2013, I oversaw the work package for the Design Flow for Silicon Photonics in the European project Plat4M. A major gap at the time in the design flow for Silicon Photonics was the lack of OPC for curvilinear design. For that reason, I join the OPC team in 2015. It led me to develop OPC solutions for Curvilinear and carry studies of OPC for EUV lithography and today High NA EUV lithography.