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Dr. Lo received his Ph.D. from National Taiwan University and joined Industrial Technology Research Institute(ITRI) in 1997. Currently, He is deputy general director and senior principal engineer in Electronic and Optoelectronic System Research Laboratories (EOSL) of ITRI and visiting Professor in Graduate School of Advanced Technology, National Taiwan University(NTU). He serves as Executive Secretary of AI on Chip Taiwan Alliance(AITA), Vice chairman of 3D IC/Panel Fan-Out consortium (Ad-STAC, Hi-CHIPS, Taiwan).

He has published more than 85 papers and 27 patent granted. His research interests focusing on the following topics, such as Semiconductor Device, Wafer-level System Integration and Advanced electronic/opto-electronic packaging for more than 20 years, including Non-Volatile Memory(MRAM, Computing in Memory), 3D IC/ 3D SiP/ 3D Chiplets Integration, Silicon Photonics & Co-packaged Optics, WBG Power chip(GaN, SiC & Ga₂O₃), Power packaging and Power module, RF packaging(Antenna-in-package, AiP), and Integrated smart system and Heterogeneous Integration technology.

He has received several awards including “Fellow of IMAPS 2024”, “Chenming Hu Award-Semiconductor device, material and process Innovation Award@VLSI-TSA 2024”, “Industry Contribution Award” by SEMI Taiwan(2023/2022), “Outstanding Engineer Award”(2021), “National Manager Excellence Award”(2018), “Innovation Elite Award”(2015) and “ITRI Elite”(2013”).